Chemical Analysis and Thermal Curing Effects of CVD graphene during Transfer Process

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Graphene has been studied due to its fascinating electrical and mechanical properties[1]. The large synthesis of graphene films by chemical vapor deposition (CVD) is expected to enable various applications such as graphene FET and transparent conducting films useful for flexible/stretchable electronics. However, the layer transfer process[2] of CVD growth graphene from metal to dielectric substrates has a practical limitation in use of CVD graphene because of chemical and mechanical stresses during transfer process.

In this work, we have studied each transfer step during whole transfer process of CVD graphene to identify the performance degradation factors and thereby to improve the electrical performance of graphene. Using XPS analysis on graphene surface, graphene by CVD growth has similar results with mechanically exfoliated graphene. However, transferred to dielectric substrate graphene shows O=C-OH bonding in XPS analysis which is induced by Cu etching step in transfer process. The O=C-OH bonding on graphene surface is strongly related to mobility degradation and electrical performance of graphene. This bonding can be removed by an thermal annealing process at 350℃ in high vacuum, H_2 or Ar gas ambient. The removal of O=C-OH bonding can improves the mobility about 30% and decrease the resistivity of graphene. These results implies that the creation of O=C-OH bonding on graphene has to be well controlled during transfer process.

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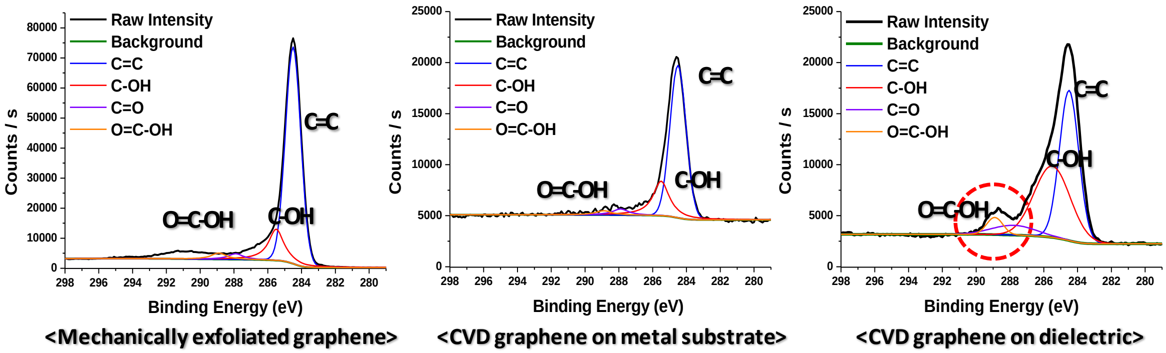
References

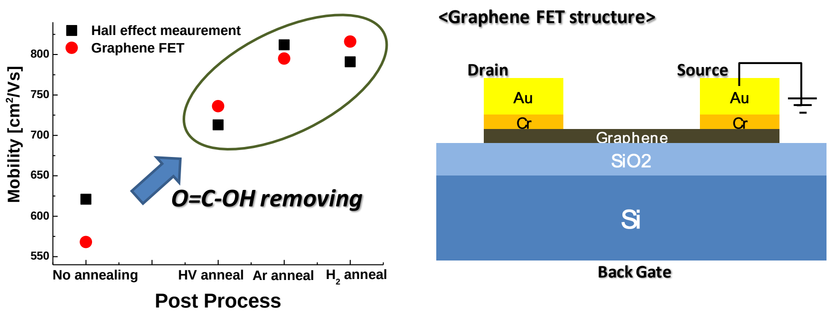
[1] K.S. Novoselov, et al. *Nature*, **438** (2005), 197

[2] X.S. Li, et al. *Nano Lett*, **9** (2009), 4359

Figures



XPS analyses on the large-scale graphene films grown by CVD after each step. (a) A mechanically exfoliated graphene film on a silicon dioxide substrate for a reference. (b) A monolayer graphene grown by CVD on a Cu substrate and (c) After the transfer to a dielectric substrate.



Electrical properties of the transferred graphene after the post annealing process. (a) Mobility variation using a back-gate transistor and the hall-effect measurement, and (b) FET structure using mobility measurement.